Claim 10 (*Original*): The sidewall dielectric forming method of Claim 9 and further wherein said plurality of exposed material layers of the ONO-type memory cell stack includes:

(b.4) a second silicon layer;

(b.5) a second silicon oxide layer;

(b.6) a tunnel dielectric layer;

(b.7) wherein the first silicon nitride layer is interposed between the first and second silicon oxide layers; and

(b.8) wherein the combination of the first and second silicon oxide layers and the first silicon nitride layer is interposed between the first and second silicon layers.

Claim 11 (*Original*): The sidewall dielectric forming method of Claim 10 and further wherein said plurality of exposed material layers of the ONO-type memory cell stack includes:

(b.9) a second silicon nitride layer; disposed above the first silicon layer.

Claim 12 (*Original*): The sidewall dielectric forming method of Claim 1 and further wherein:

a height evaluation ratio, $R_H = H_{outer}/H_{inner}$, determined for the ONO-type memory cell stack after formation of the sidewall dielectric by the dry ISSG process, is about 1.20 or less, where H_{inner} represents a stack height at a lateral position in the stack that is spaced away from the stack edges and where H_{outer} represents a stack height at a lateral position near or at one of the stack edges.

Claim 13 (*Original*): The sidewall dielectric forming method of Claim 1 and further wherein lateral sidewall breakdown voltages are substantially uniform along the height of the ONO-type memory cell stack after formation of the sidewall dielectric by the dry ISSG process.

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MacPherson, Kwok, Chen & Heid LLP
1762 Technology Drive
Suite 226
San Jose, CA 95110
Telephone (408) 392-9520
Fax (408) 392-9262

Claim 14 (*Original*): The sidewall dielectric forming method of Claim 1 and further wherein a larger erase speed is obtained in a memory cell having said ONO-type memory cell stack after formation of the sidewall dielectric by the dry ISSG process, where the larger erase speed is larger than a corresponding erase speed obtained in a corresponding memory cell having an ONO-type memory cell stack with sidewall dielectric formed by an HTO process.

Claim 15 (*Original*): The sidewall dielectric forming method of Claim 1 and further comprising:

(b) after said dry ISSG process, forming further and supplemental sidewall dielectric by a non-ISSG sidewall dielectric forming process.

Claim 16 (*Withdrawn*): A memory cell having an ONO-type memory cell stack where at least one sidewall of the ONO-type memory cell stack includes a plurality of material layers respectively composed of different materials, the memory cell further comprising:

(a) a sidewall-coating dielectric whose fabrication was at least initially started by subjecting at least one otherwise exposed and multi-layered sidewall of the ONO-type memory cell stack to a dry ISSG process (In-Situ Steam Generation).

Claim 17 (*Withdrawn*): The memory cell of Claim 16 wherein the dry ISSG process used to fabricate the memory cell comprises:

(a.1) generating a sufficient amount of atomic oxygen near said at least one otherwise exposed sidewall of the ONO-type memory cell stack so as to substantially oxidize exposed sidewall regions of those of the different materials of the ONO-type memory cell stack that are not substantially oxidized prior to said subjecting of the at least one otherwise exposed sidewall to said dry ISSG process.

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MacPherson, Kwok, Chen & Heid LLP
1762 Technology Drive
Suite 226
San Jose, CA 95110
Telephone (408) 392-9520
Fax (408) 392-9262

Claim 18 (*Withdrawn*): The memory cell of Claim 16 wherein the oxidation process used to fabricate the memory cell comprises:

(a.1) flowing molecular oxygen (O_2) towards the stack; and

(a.2) flowing molecular hydrogen (H_2) towards the stack, where the volumetric flow ratio of the H_2 to the O_2 is less than about 0.2.

Claim 19 (*Withdrawn*): A memory cell having an ONO-type memory cell stack isolated by sidewall dielectric where at least one dielectric-isolated sidewall of the ONO-type memory cell stack includes a plurality of material layers respectively composed of different materials, the memory cell being further characterized by :

(a) a height variation ratio, $R_H = H_{outer}/H_{inner}$, determined for the ONO-type memory cell stack after formation of the sidewall dielectric, where the height variation ratio, R_H is about 1.20 or less, where H_{inner} represents a stack height at a lateral position in the stack that is spaced away from the stack edges and where H_{outer} represents a stack height at a lateral position near or at one of the stack edges.

Claim 20 (*Withdrawn*): A memory cell having an ONO-type memory cell stack isolated by sidewall dielectric where at least one dielectric-isolated sidewall of the ONO-type memory cell stack includes a plurality of material layers respectively composed of different materials, the memory cell being further characterized by :

(a) lateral sidewall breakdown voltages that are substantially uniform along the height of the ONO-type memory cell stack.

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LAW OFFICES OF
MacPherson, Kwok, Chen & Heid LLP
1762 Technology Drive
Suite 226
San Jose, CA 95110
Telephone (408) 392-9250
Fax (408) 392-9262